

SCS:lam 6319-56134 144728 10/03/02

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Total No. Pages: 6 including this cover sheet

Message: Transmitted herewith for filing in the above-identified application is an Amendment After Final Rejection. If you do not receive all pages or if you have problems receiving transmittal, please call Stacey C. Slater at (503) 226-7391.

In re application of: Chang, Chin-Huang

Application No.: 09/660,753

Filed: September 13, 2000

For: METHOD FOR REDUCING SIZE OF
SEMICONDUCTOR UNIT IN PACKAGING
PROCESS

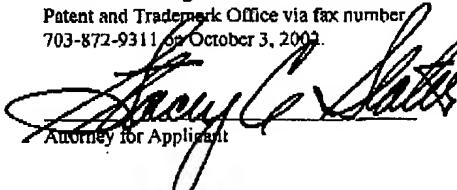
Examiner: Lan Vinh

Art Unit: 1756

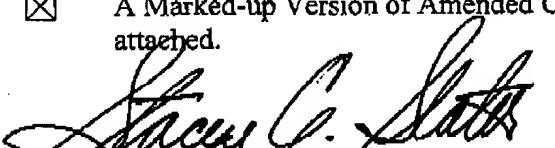
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Stacey C. Slater
Attorney for Applicant

- No additional fee is required.
- Please charge any fees that may be required in connection with filing this amendment and any extension of time, or credit any overpayment, to Deposit Account No. 02-4550. A copy of this sheet is enclosed.
- A Marked-up Version of Amended Claims Pursuant to 37 C.F.R. §§ 1.121(b)-(c) is attached.



Stacey C. Slater
Registration No 36,011

October 3, 2002

Date

cc: Docketing

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SCS:lam 10/3/02 144712
PATENTAttorney Reference Number 6319-56134
Application Number 09/660,753

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Response Under 37 C.F.R. § 1.116 Expedited Procedure

In re application of: Chang, Chin-Huang

Art Unit: 1756

Application No. 09/660,753

Filed: September 13, 2000

For: METHOD FOR REDUCING SIZE OF
SEMICONDUCTOR UNIT IN
PACKAGING PROCESS

Examiner: Lan Vinh

Date: October 3, 2002

COMMISSIONER FOR PATENTS

Washington, DC 20231

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addressed to COMMISSIONER FOR PATENTSStacy L. Slaten
Attorney for ApplicantCERTIFICATE OF FACSIMILE

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AMENDMENT AFTER FINAL REJECTION

This responds to the Advisory Action dated September 20, 2002, concerning the application referenced above. Please amend the application as follows.

In the Claims:

Please amend the claims as follows.

1. (Amended) A method for reducing the size of at least a semiconductor unit in a process of making a package including a carrier and said semiconductor unit, said semiconductor unit including a first surface and a second surface, said second surface having no electrical connection device thereon, said method comprising:

attaching at least a part of said first surface to said carrier; and

etching said semiconductor unit from said second surface to reduce semiconductor unit